CLAIMS:

1. A linear amplifier circuit comprising:

- a first differential amplifier (DA1) having a differential input terminals (I+, I-) for receiving a binary input signal, and a differential output terminals (O+,O-),

- a second differential amplifier (DA2) having input terminals coupled to the differential input terminals (I+, I-),

- a third differential amplifier (DA3) coupled in cascade to the second differential amplifier (DA2) and having its output cross-coupled to the differential output terminals in a feed-forward connection, and

- a capacitor (C) coupled to the third differential amplifier (DA3) for determining an increase of a bandwidth of the linear amplifier, a current flowing through the capacitor (C) being proportional with a derivative of the differential input signal (I+, I-).

2. A linear amplifier as claimed in claim 1, wherein the first differential amplifier (DA1) comprises a first transistor pair (M1, M6) coupled to a common drain transistor pair (M3, M4) via resistor means (R), a current through the common drain transistor pair (I3) improving a linearity of the first differential amplifier (DA1).

3. A linear amplifier as claimed din claim 1, wherein the second differential amplifier (DA2) comprises a second transistor pair (M2, M5) being supplied with a substantially equal current as the first differential amplifier (DA1).

4. A linear amplifier as claimed in claim 1, wherein the third differential amplifier (DA3) comprises a third transistor pair (M7, M8) having their respective source terminal coupled via the capacitor (C).

5. A limiter amplifier comprising:

- a chain of linear amplifier circuits (LIN1, LIN2, LIN3, LIN4) as claimed in claim 1,

- a plurality of limiting amplifiers (NLN1, NLN2, NLN3, NLN4) coupled in cascade and further coupled to the chain of linear amplifiers (LIN1, LIN2, LIN3, LIN4) and providing a limited differential signal (OUT+, OUT-).

6. A limiter amplifier as claimed in claim 5 further comprising a feedback differential integrator (A1, R1, R2, R3, R4, C1, C2) for adjusting an offset voltage of the limiter amplifier.

7. A limiter amplifier as claimed in claim 5 wherein at least one of the limiting amplifiers (NLN4) of the plurality of limiting amplifiers (NLN1, NLN2, NLN3, NLN4) has input terminals coupled via series coupled substantially equal resistors (R0) for providing a common mode signal (VCM).

8. A limiter amplifier as claimed in claim 7 further comprising a replica biasing circuit providing a compensation signal (Icomp) biasing the chain of linear amplifiers (LIN1, LIN2, LIN3, LIN4) and the plurality of limiting amplifiers (NLN1, NLN2, NLN3, NLN4).

9. A limiter amplifier as claimed in claim 8, wherein the replica biasing circuit comprises:

- a pair of replica transistors (MR1, MR2) having coupled their respective terminals i.e. drain to drain, source to source and gate to gate, their gates being coupled to the common mode signal, and

- a transconductance amplifier (A2) generating the compensation signal (Icomp) which is proportional with a difference between a reference signal (VSW) and a voltage in the drains of the of the pair of replica transistors (MR1, MR2).